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A Study of the Intermetallic Compound Growth in Flip-Chip Packages under Thermal Loading

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Abstract: The intermetallic compound layers in solder bumps have the brittle feature and can easily fracture under thermal or mechanical loading. Therefore, the intermetallic compound is an issue for the fracture reliability of the solder bumps. In this work, the intermetallic compound growth before and after high temperature storage tests was investigated. The experiment results revealed that the solder bumps with nickel layers could reduce the intermetallic compound growth rate. The nickel layer, which was added in between Cu and SnAg for top solder bumps, was an important factor controlling the intermetallic compound thickness. It was hard to tell the intermetallic compound thickness at time zero; at the time of 147 hours, the intermetallic compound grew to 3.25 μm; at the time of 294 hours, the intermetallic compound grew to 5.25 μm. However, the solder joints were still in good condition.
Keywords: Intermetallic compound; Thermal loading; Fracture reliability; Solder joint.

1. Introduction

Nowadays the semiconductor chips demand smaller packages and higher functionality, which requires the chips to have more inputs/outputs. The bump height and pitch must be reduced in order to fulfill this requirement. The initial wafer-level packaging is known as the wafer-level chip-scale packaging technology [1]. The fan-out wafer-level package technology [2] is a further development of the wafer-level chip-scale packaging technology [3, 4], and its most significant aspect is the fan-out area [5, 6]. The fan-out wafer-level package input/output numbers are much higher than the wafer-level chip-scale packaging input/output numbers. The fan-out wafer-level packages [7, 8] can be further developed to 2.5D/3D fan-out wafer-level packages [9, 10] or fan-out package-on-package [11, 12] through laser ablation or through silicon via (TSV) technology.

The silicon die must be thin so as to build a thin over-molded [13] structure fan-out wafer-level package [14]. The fan-out wafer-level package also shows better thermal-mechanical reliability performance [15, 16] than other packages such as plastic ball grid array packages [17]. The next generation wafer level packaging turns to panel carrier [18], and thus the yield will increase exponentially and the cost will reduce significantly [19]. The three-point bending test [20] is the most popular method for the evaluation of silicon strength. Some research has shown that the silicon own profile factors do not affect the silicon strength obviously and directly [21, 22]. There are three widely accepted effect factors of silicon strength: silicon surface defects, silicon edge defects and weak planes of silicon crystal lattice [23].

Compared with other flip chip technologies [24, 25], three-dimensional chip stacking packaging with micro bumps has many advantages: better electrical performance, shorter interconnect lengths, thinner package profile, and enhanced function density. Zhan et al. [26] proposed a high-density three-dimensional chip-on-chip packaging technology with lead-free solder micro-bump interconnections. In their work, they used underfill dispensing and thermal compression bonding processes and assembled a number of Cu/Ni micro-bumps on an interposer or silicon chip with Sn2.5Ag solders.

However, many issues remain to be addressed before the technology can be feasible. The shorter bump height and fine pitch can benefit the atomic diffusion, but the intermetallic compound layer in the solder joint has a serious effect on the solder joint fracture reliability and thus the whole package reliability. The intermetallic compound is very brittle and may fracture under certain thermal or mechanical loading. Therefore, a thick intermetallic compound layer is a potential problem to the package reliability. A foreign material layer may prevent the copper from its reaction with tin [27]. A thin intermetallic compound layer of a few micrometres thick could create a good metallurgical bonding strength [28]. The foreign material layer might prevent the intermetallic compound growth [29-31].

One research [32] found that the solder bump standoff height was a factor that could affect the solder joint reliability. The researchers conducted the research through mathematics prediction calculation, experiment and FEM etc. The research was very detailed, but the conclusions stated that the solder bump standoff height was not critical to the intermetallic compound formation. This point was verified by a solder bump material study [33]. Cu and Ni atoms could cross hundreds of micrometres in a few hundred hours to interact with other atoms even in the solid state. The solder bump topology was an important factor, which affected the intermetallic compound formation. This was because the thermal-mechanical stress affected the fine solder bump pitch package reliability during thermal testing [34]. But, the research only showed a single solder bump pitch. There were not any comparisons between different solder bump pitches within the same package.

Another research [35] showed the function of a Ni layer for 100-μm and 200-μm micro bump pitches could prevent the intermetallic compound growth effectively. But, the bump pitches were not fine pitches. The solder bump topology might accelerate the intermetallic compound formation. However, the solder bump material was the source of intermetallic compound layers, and resulted in the intermetallic compound layer formation difficulty. The tin/silver/copper (SAC) solder alloy is the most popular selection of packaging manufacturers. The Ag content in SAC solder bumps affects the Ag3Sn intermetallic compound formation [36, 37]. According to atom chemistry properties, the reaction between some atoms requires higher energy. Heat is the source of energy. Therefore, the intermetallic compound layer formation always occurs in heat-related processes, like the reflow process and thermal reliability tests etc. If the external heat is not enough to break the existing chemical bond, then the new composition formation is stopped. Vice versa if the chemical bond threshold is low, then the new composition formation does not require much energy. Based on this property, the intermetallic compound growth rate may be reduced significantly through adding a foreign material in the solder bumps, like antimony (Sb) [38, 39]. Nickel (Ni) could be another foreign material to reduce the intermetallic compound growth rate [40]. However, there was not any concentrated and detailed research to show this. The shorter bump height and fine pitch can benefit the atomic diffusion. The intermetallic compound is very brittle and may fracture under certain thermal or mechanical loading. Therefore, a thick intermetallic compound layer is a potential problem to the package reliability.

In this work, the intermetallic compound growth before and after high temperature storage tests was investigated, so as to study the fracture reliability of the solder bumps with nickel layers added.

2. Methodology

The samples were 14 mm × 20 mm flip chip packages in this experiment. There were two dies with different sizes in each package. The big die had a solder bump pitch of 80 μm; the smaller die had solder bump pitches of 40 μm and 60 μm. The solder bump diameter was 20 μm. There were two batches of samples, and they were named S1 and S2 samples. Table 1 lists the solder bump composition of these samples. The materials of the top solder bumps were Cu/SnAg and Cu/Ni/SnAg. The material of the interposer side solder bumps was Cu/Ni/SnAg.

The top die was attached by using a chip attach machine with a bonding force of 4 kg and bonding time of 1 second. The whole wafer suffered a reflow process after the chip-attach process. An underfill process was applied and the underfill was cured at 180 °C for 4 hours.

Table 1. Solder bump composition of samples.

	Die side		Interposer side	
	Composition	Thickness (μm)	Composition	Thickness (μm)
S1	Cu/SnAg	25/15	Cu/Ni/SnAg	3/3/5
S2	Cu/Ni/SnAg	25/3/15	Cu/Ni/SnAg	3/3/5

The conditions of the accelerated high temperature storage test were almost the same as that of the normal high temperature storage test, but the tested devices were stored at a higher temperature. The temperature of the accelerated high temperature storage test was 175 °C, which was higher than 150 °C for the normal high temperature storage test. There were 50 confirming units (ten each from top, left, center, right and bottom) selected from each wafer for the high temperature storage test. The readout points were 147 hours and 294 hours. Two samples were taken out at each readout point, and cross sectioning was performed for the samples with 40, 60 and 80 μm solder joint pitches. We also selected some time-zero samples for comparison purposes. The samples were polished without the cold mount. A scanning electron microscope was utilised to observe the microstructure of the intermetallic compound and make the measurement.

3. Experiment results

Figure 1 shows an image of a solder joint condition of an S1 sample at time zero. There is a clear thickness difference of the intermetallic compound layers on the two sides of the bump. The die (top) side intermetallic compound layer thickness is about 3 μm, but the interposer-side intermetallic compound layer is difficult to observe. The die-side copper column is etched by the intermetallic compound layer and its shape is changed. However, the copper and nickel layers still keep their shapes on the interposer-side of the solder.

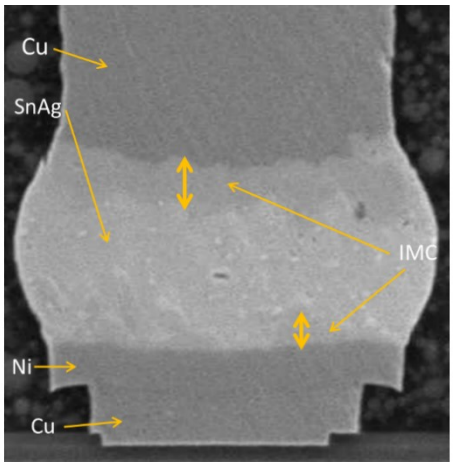

Figure 1. A solder joint of an S1 sample at time zero without a nickel layer on the top-side.

Figure 2 shows the cross-section images of sample-S1 solder joints after the 147 hours and 294 hours accelerated high temperature storage test. After the 147 hours accelerated high temperature storage test, the die (top) side intermetallic compound layers almost grew twice compared with time-zero samples. However, the interposer-side intermetallic compound layers grew only a little from 'difficult to observe' to 'can be observed'. For the 80-μm pitch, the intermetallic compound growth rate was the fastest among the three pitches, and the top and bottom intermetallic compound layers almost joined together. The die-side intermetallic compound layers etched the copper column continuously, and the copper column shape became trapezia from rectangles. The copper column thickness was also reduced. This means that more Cu atoms participated in the intermetallic compound formation.

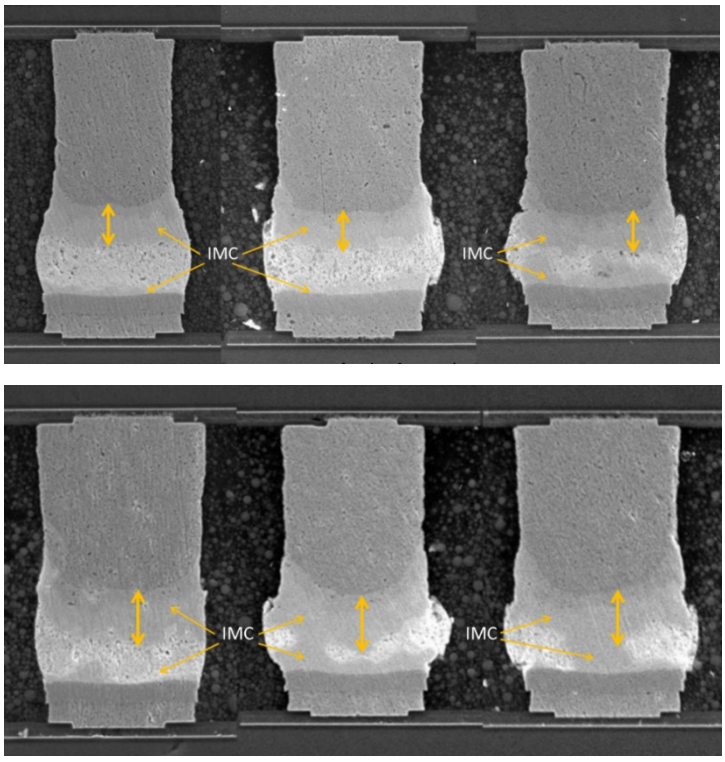

Figure 2. The cross-section images of sample-S1 solder joints with 40, 60 and 80 μm pitches after 147 hours (top) and 294 hours (bottom) accelerated high temperature storage tests.

After the 294 hours accelerated high temperature storage test, the die (top) side intermetallic compound layers grew continuously and rapidly. They took up the dominant solder joint space. For the 60 and 80 μm pitches, their top and bottom intermetallic compound layers joined together and became integrated. For the 40 μm pitches, their top and bottom intermetallic compound layers almost joined together. Anyway, the top side intermetallic compound layers were the major contributor. The die-side intermetallic compound layers etched the copper column continuously, and the copper column shape became rounds from trapezia. The copper column thickness was also reduced further. For the interposer-side solder joints, their Cu and Ni layers, especially the Cu layers, still retained their shapes.

According to the above observations, Ni has an obvious effect on the intermetallic compound growth. The die side intermetallic compound layers (without Ni) always grow rapidly and take up the major solder joint space. However, the interposer side intermetallic compound layers (with Ni) grow slowly, and they merge with die side intermetallic compound layers passively.

According to the above experiment results, the intermetallic compound growth rate on the interposer side was much slower than that on the die side. This might be because of the nickel layer of the interposer-side solder bump. Therefore, a 3-μm nickel layer was added in the die-side solder bumps of S2 samples. We expected that this nickel layer could reduce the die-side intermetallic compound growth.

Figure 3 gives the cross-section images of the solder joints before the reliability test for three different pitches of S2 samples. There is a nickel layer added in the die (top) side solder bump, and hence the composition of the die-side solder bump is Cu/Ni/SnAg. The nickel layer can prevent the SnAg compound from climbing up and reduce the chance of Cu, Sn and Ag compound formation.

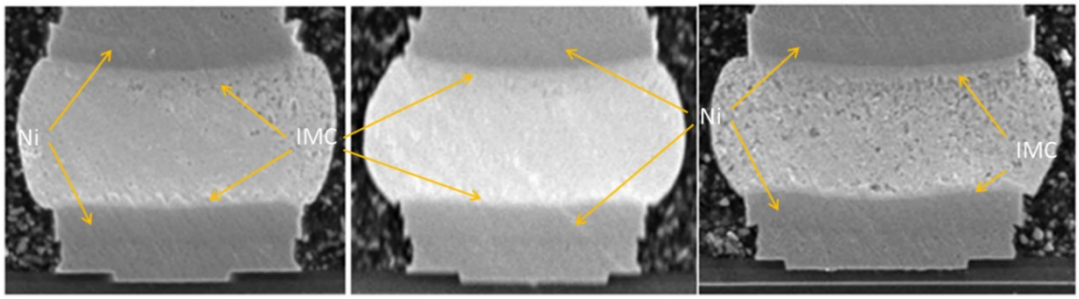

Figure 3. The cross-section images of solder joints with 40, 60 and 80 μm pitches (with nickel layers on both sides) at time zero.

Figure 4 shows the images of the solder joints after 147 hours and 294 hours accelerated high temperature storage tests. The intermetallic compound layers grow up continuously throughout the tests; however, the test result is much better than that shown in Figure 2. No any intermetallic compounds join together after the 294 hours accelerated high temperature storage test. No any intermetallic compounds appear in the copper column of top-side solder bumps after the 147 hours accelerated high temperature storage test, and the nickel layer prevents the intermetallic compound growth successfully at this time point. The thickness of intermetallic compound layer is 3.25 μm after the 147 hours accelerated high temperature storage test, and 5.25 μm after the 294 hours accelerated high temperature storage test. The intermetallic compound layers grew 2 μm after 147 hours of accelerated high temperature storage testing. However, the solder joints were in good condition, and they were still functional.

4. Conclusions

This experimental study revealed that the nickel layer, which was added in between Cu and SnAg for top-side solder bumps, was an important factor controlling the intermetallic compound thickness. It has proved that the nickel layer has an effective impact on the intermetallic compound thickness. We applied accelerated high temperature storage tests to the samples for 147 and 294 hours respectively at 175 °C. It was hard to tell the intermetallic compound thickness at time zero; at the time of 147 hours, the intermetallic compounds grew to 3.25 μm; at the time of 294 hours, the intermetallic compound grew to 5.25 μm. However, the solder joints were still in good condition. Moreover, the intermetallic compound growth rate remained the same regardless the solder bump composite.

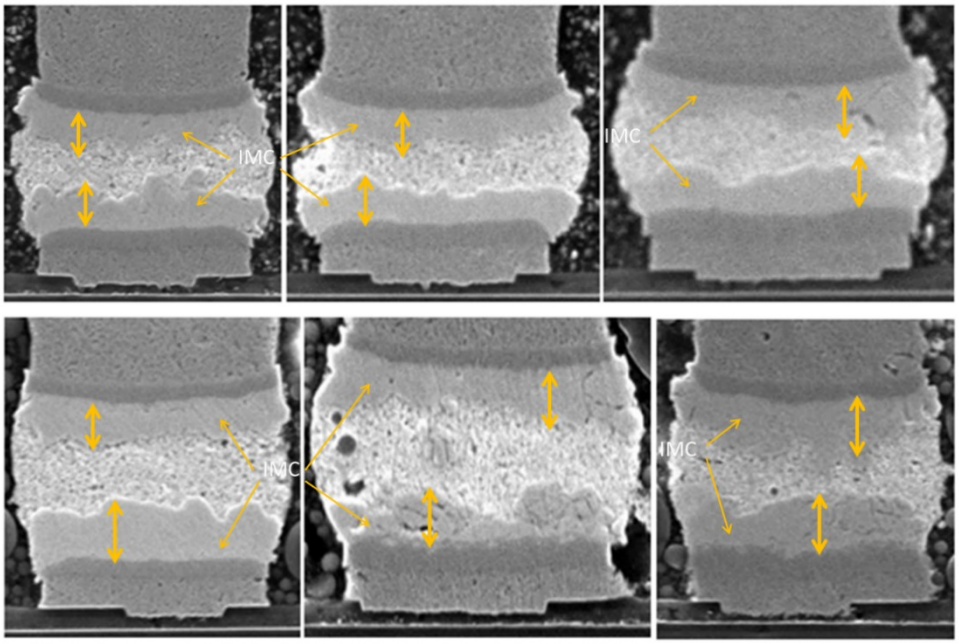

Figure 4. The cross-section images of sample-S2 solder joints with 40, 60 and 80 μm pitches (with nickel layers on both sides) after 147 hours (top) and 294 hours (bottom) accelerated high temperature storage tests.

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